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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/073,241	02/13/2002	Marko Karppanen	1154.41135X00	8874

20457 7590 11/02/2005

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EXAMINER	
MCCARTHY, CHRISTOPHER S	

ART UNIT	PAPER NUMBER
2113	

DATE MAILED: 11/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/073,241	KARPPANEN, MARKO	
	Examiner	Art Unit	
	Christopher S. McCarthy	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 9-16, 19-23, 25, and 27 are rejected under 35 U.S.C. 102(e) as being anticipated by Golikeri et al. U.S. Patent Application Publication US2003/0067926.

As per claim 9, Goliekeri teaches a method for improving the reliability of a computer system including a bus, and plug-in units coupled thereto (paragraph (P) 0036), comprising: providing to each of plural plug-in unit a s separate interface circuit such that each of said plug-in unit is connected to said bus via said interface circuit corresponding thereto (P 0036); addressing a respective plug-in unit, via the bus, by addressing operations directed at said respective plug-in unit and which are monitored by interface circuit corresponding thereto (P 0039); performing a time duration operation of addressing of said plug-in unit (P 0039); and checking the state of addressing of the addressed plug-in unit such that (i) when the addressing is ended before expiration of a predetermined period of time, the time duration operation of

addressing is terminated and a new time duration operation of addressing is set to commence at time of next occurrence of addressing (P 0041), and (ii) when the duration operation of addressing exceeds the predetermined time period, the addressing to that plug-in unit is terminated by said interface circuit corresponding thereto by sending into the bus a signal indicating termination of addressing (P 0039).

As per claim 10, Goliekeri teaches a method as defined in claim 9, wherein: the time duration of addressing is monitored using a watchdog timer with a predetermined timing set therein (P 0041).

As per claim 11, Goliekeri teaches a method as defined in claim 9, wherein: when addressing is terminated an error signal is set by the interface circuit into an active state in the bus (P 0039; wherein, when the address is purged, upon an error, a purge message is sent on the bus).

As per claim 12, Golikeri teaches a method as defined in claim 9, wherein: when addressing is terminated an error signal indicating an error condition in the plug-in unit is set by the interface circuit into active state in the status register of the plug-in unit (P 0040, 0041; wherein, the status of the register is inherently changed in that the module will no longer send out "keep-live" messages to other modules, so they will know that the address was purged, Just in case the purge message was not received by all other modules).

As per claim 13, Golikeri teaches an interface circuit for providing local monitoring capability to a plug-in unit of a computer system including a bus; and plug-in units coupled to said bus; wherein a separate interface circuit is provided to connect each of said plug-in unit to said bus (P 0036) and comprising: a watchdog timer (P 0039, 0041); first means for activating

the watchdog timer upon start of an addressing operation directed to the plug-in unit corresponding thereto, and second means for sending into the bus a signal indication termination of addressing, the termination of addressing being effected when the duration of said addressing exceeds a predetermined time duration for addressing, as measured by the watchdog timer (P 0039).

As per claim 14, Golikeri teaches an interface circuit as defined in claim 13, further comprising: means for setting an error signal into active state in the bus (P 0039).

As per claim 15, Golikeri teaches an interface circuit as defined in 13, further comprising: for setting a signal indicating an error condition in the plug-in unit into an active state in the status register of the plug-in unit (P 0040, 0041; wherein, the status of the register is inherently changed in that the module will no longer send out "keep-live" messages to other modules, so they will know that the address was purged, Just in case the purge message was not received by all other modules).

As per claim 16, Golikeri teaches an interface circuit as defined in 14, further comprising: for setting a signal indicating an error condition in the plug-in unit into an active state in the status register of the plug-in unit (P 0040, 0041; wherein, the status of the register is inherently changed in that the module will no longer send out "keep-live" messages to other modules, so they will know that the address was purged, Just in case the purge message was not received by all other modules).

As per claim 19, Golikeri teaches an interface circuit as defined in claim 13, wherein each said interface circuit is provided as a part of said plug-in unit corresponding thereto (P 0036-0039; fig. 2).

As per claim 20, Golikeri teaches a method according to claim 10, wherein: said watchdog timer is provided at each said interface circuit or at each said plug-in unit (P 0039, 0041).

As per claim 21, Golikeri teaches a computer system including a bus and at least one plug-in unit coupled thereto, wherein the improvement comprises: providing a plurality of interface circuit and a plurality of one plug-in unit each of which is connected to said bus via a separate said interface circuit corresponding thereto (P 0036), wherein each said interface circuit comprises a watchdog timer (P 0039, 0041), first means for activating the watchdog timer upon start of an addressing operation directed to the plug-in unit corresponding thereto, and second means for sending into the bus a signal indicating termination of addressing, the termination of addressing being effected when the duration of said addressing exceeds a predetermined time duration for addressing, as measured by the watchdog timer (P 0039).

As per claim 22, Golikeri teaches a computer system according to claim 21, wherein each said interface further comprises: means for setting an error signal into an active state in the bus (P 0039).

As per claim 23, Golikeri teaches a computer system according to claim 22, wherein each said interface circuit comprises means for setting a signal indicating an error condition in the corresponding plug-in unit into an active state in a status register of the plug-in unit (P 0040, 0041; wherein, the status of the register is inherently changed in that the module will no longer send out "keep-live" messages to other modules, so they will know that the address was purged, Just in case the purge message was not received by all other modules (P 0040, 0041; wherein, the status of the register is inherently changed in that the module will no longer send out "keep-live"

messages to other modules, so they will know that the address was purged, Just in case the purge message was not received by all other modules).

As per claim 25, Golikeri teaches a computer system according to claim 21, wherein each said interface circuit comprises means for setting a signal indicating an error condition in the plug-in unit into an active state in a status register of the plug-in unit (P 0040, 0041; wherein, the status of the register is inherently changed in that the module will no longer send out "keep-live" messages to other modules, so they will know that the address was purged, Just in case the purge message was not received by all other modules).

As per claim 27, Golikeri teaches a computer system according to claim 21, wherein each said interface circuit is provided as a part of said plug-in unit corresponding thereto (P 0036-0039, Figure 2).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 17-18, 24, 26, 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Golikeri in view of Microsoft Computer Dictionary, referred hereon as Microsoft.

As per claim 17, Golikeri teaches an interface circuit as defined in claim 13 with a bus (P 0036). Golikeri does not explicitly teach wherein the bus is a CompactPCI bus. Microsoft does teach a CompactPCI bus (page 99). It would have been obvious to one of ordinary skill in the art

at the time the invention was made to use the CompactPCI bus of Microsoft in the bus system of Golikeri. One of ordinary skill would have been motivated to use the CompactPCI bus of Microsoft in the bus system of Golikeri because Microsoft teaches wherein the CompactPCI bus is suitable for high-speed communication devices, such as router; this is an explicit embodiment of Golikeri (0088), and a high speed communication means would have been a desired advantage in Golikeri in that he teaches the desire of multiple connected peripheral modules, such as routers, in strict synchronization with another.

As per claim 18, Golikeri teaches an interface circuit as defined in claim 16 with a bus (P 0036). Golikeri does not explicitly teach wherein the bus is a CompactPCI bus. Microsoft does teach a CompactPCI bus (page 99). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the CompactPCI bus of Microsoft in the bus system of Golikeri. One of ordinary skill would have been motivated to use the CompactPCI bus of Microsoft in the bus system of Golikeri because Microsoft teaches wherein the CompactPCI bus is suitable for high-speed communication devices, such as router; this is an explicit embodiment of Golikeri (0088), and a high speed communication means would have been a desired advantage in Golikeri in that he teaches the desire of multiple connected peripheral modules, such as routers, in strict synchronization with another.

As per claim 24, Golikeri teaches a computer system according to claim 23, with a bus (P 0036). Golikeri does not explicitly teach wherein the bus is a CompactPCI bus. Microsoft does teach a CompactPCI bus (page 99). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the CompactPCI bus of Microsoft in the bus system of Golikeri. One of ordinary skill would have been motivated to use the CompactPCI bus of

Microsoft in the bus system of Golikeri because Microsoft teaches wherein the CompactPCI bus is suitable for high-speed communication devices, such as router; this is an explicit embodiment of Golikeri (0088), and a high speed communication means would have been a desired advantage in Golikeri in that he teaches the desire of multiple connected peripheral modules, such as routers, in strict synchronization with another.

As per claim 26, Golikeri teaches a computer system according to claim 21, with a bus (P 0036). Golikeri does not explicitly teach wherein the bus is a CompactPCI bus. Microsoft does teach a CompactPCI bus (page 99). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the CompactPCI bus of Microsoft in the bus system of Golikeri. One of ordinary skill would have been motivated to use the CompactPCI bus of Microsoft in the bus system of Golikeri because Microsoft teaches wherein the CompactPCI bus is suitable for high-speed communication devices, such as router; this is an explicit embodiment of Golikeri (0088), and a high speed communication means would have been a desired advantage in Golikeri in that he teaches the desire of multiple connected peripheral modules, such as routers, in strict synchronization with another.

As per claim 28, Golikeri teaches a computer system according to claim 27, with a bus (P 0036). Golikeri does not explicitly teach wherein the bus is a CompactPCI bus. Microsoft does teach a CompactPCI bus (page 99). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the CompactPCI bus of Microsoft in the bus system of Golikeri. One of ordinary skill would have been motivated to use the CompactPCI bus of Microsoft in the bus system of Golikeri because Microsoft teaches wherein the CompactPCI bus is suitable for high-speed communication devices, such as router; this is an explicit embodiment

of Golikeri (0088), and a high speed communication means would have been a desired advantage in Golikeri in that he teaches the desire of multiple connected peripheral modules, such as routers, in strict synchronization with another.

Response to Arguments

5. Applicant's arguments with respect to claims 19-28 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: See attached PTO-892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher S. McCarthy whose telephone number is (571)272-3651. The examiner can normally be reached on M-F, 9 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571)272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

csm
October 28, 2005

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